

FIG 1 Section A-A

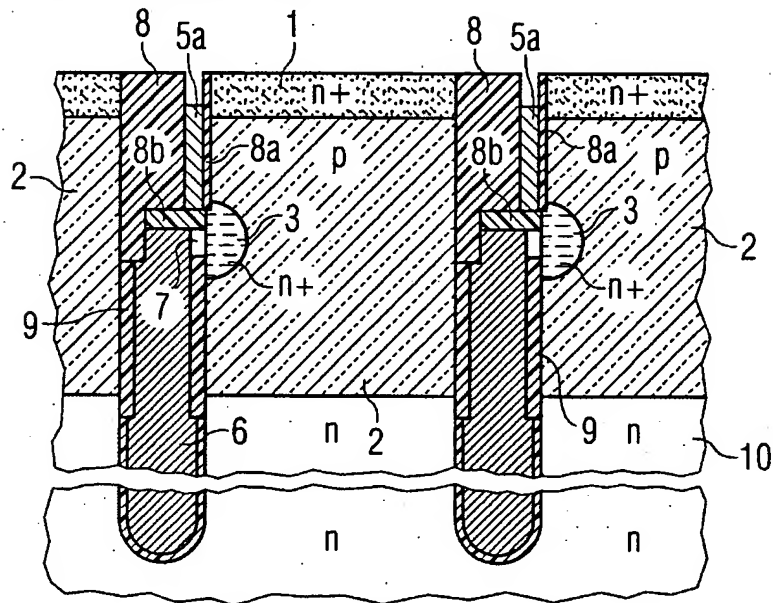
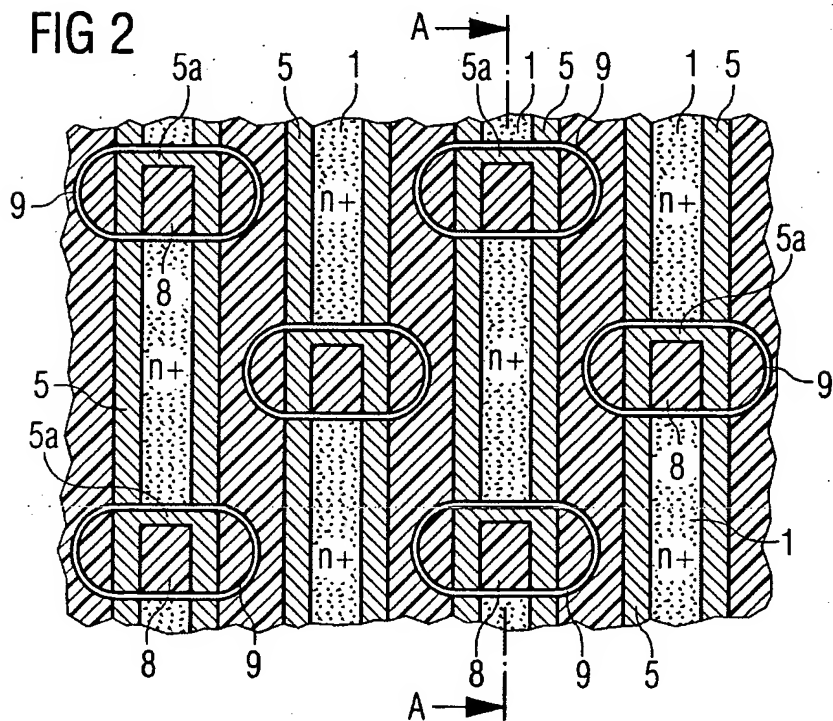


FIG 2









	Gate		p (channel area)		Isolation/ dielectric
	Webs (AT) (Source region)		Poly Si/ tungsten/WL		Drain region

FIG 3

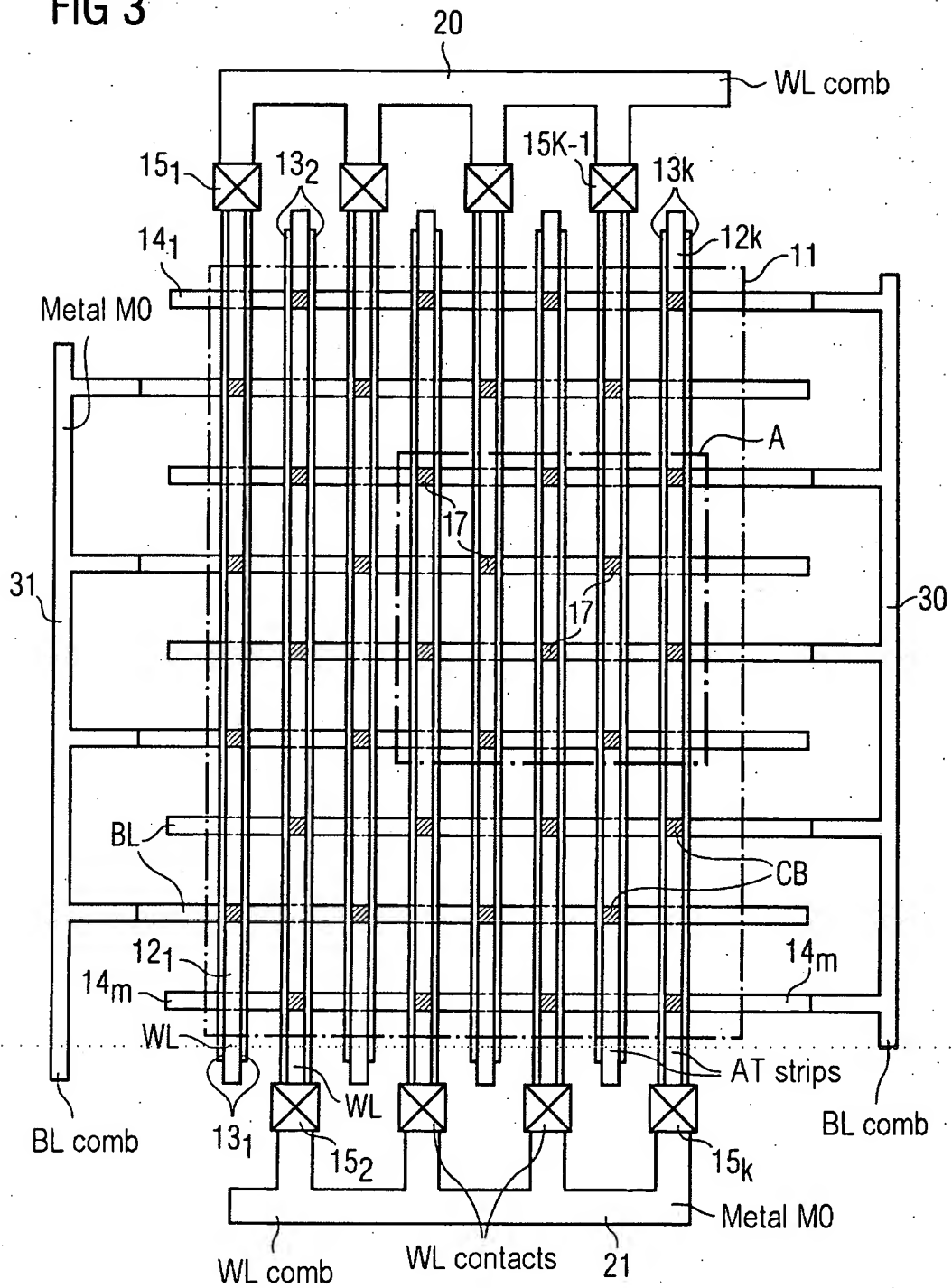


FIG 4

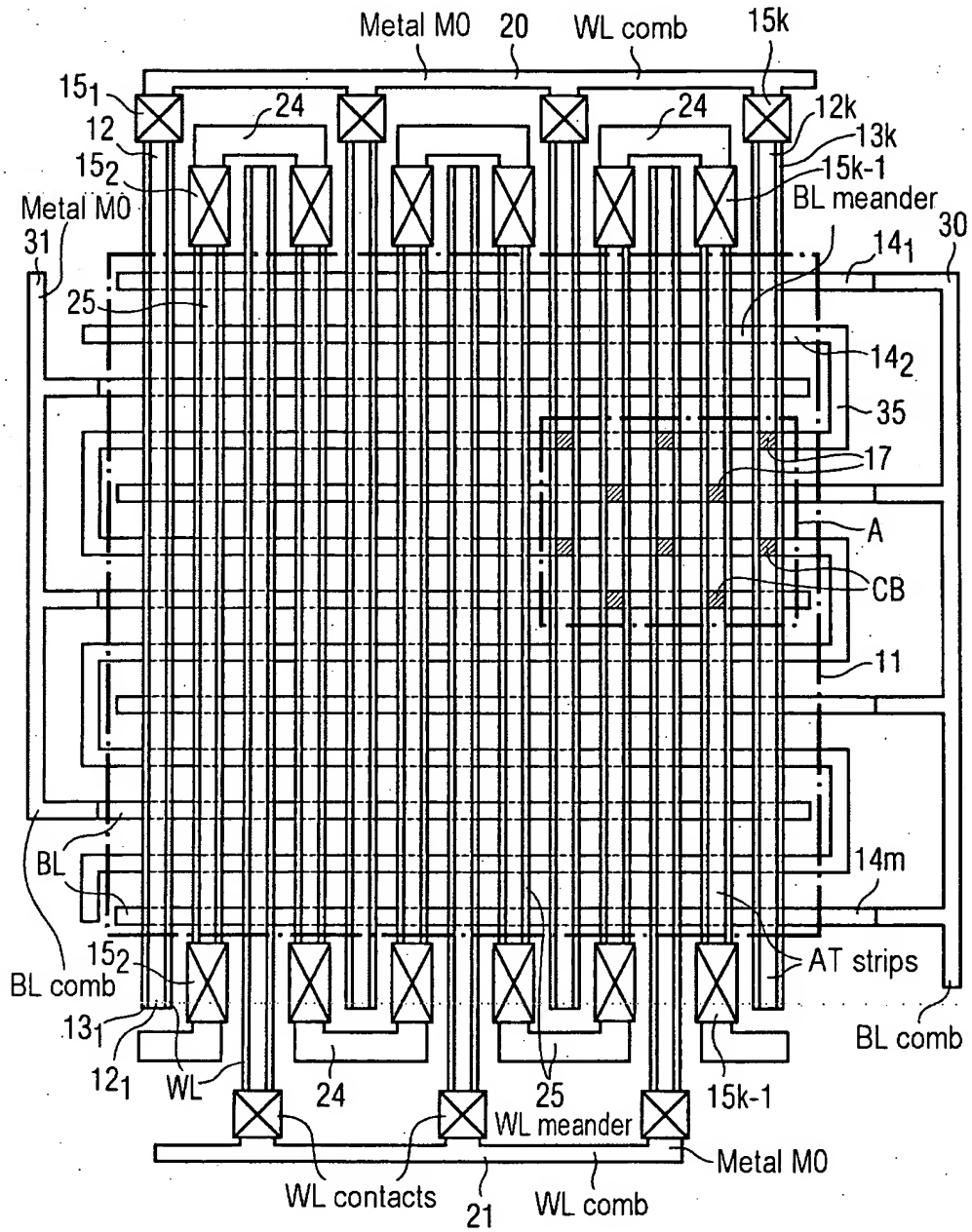


FIG 5 Detail A

